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| 10/069,229 | 12/11/2002 | Gilbert Wolrich | 10559-305US1 | 1429 |

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| EXAMINER | |
|---|---|
| JOO, JOSHUA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2154 | |

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/069,229 | WOLRICH ET AL. | |
| | Examiner | Art Unit | |
| | Joshua Joo | 2154 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Response to Amendment filed 12/29/2005***

1. Claims 1-21 are presented for examination.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6, 10, 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carron et al, US Patent #4,724,521 (Carron hereinafter), in view of Yates et al, US Patent #5,802,373 (Yates hereinafter) and White et al, US Patent #5,748,950 (White hereinafter).

4. As per claim 1, Carron teaches substantially the invention as claimed including the method of operating a processor, Carron's teachings comprise of:

executing a branch instruction that causes a processor to branch from executing a first sequential series of instructions to a different sequential series of instructions (Col 134, lines 31-32. Process is branched if the test passes or continues with operation if the test fails.) based on a byte specified by an instruction in a buffer, being equal or not equal to a specified byte value (Col 134, lines 30-31. Compares byte values to a byte value.), if the specified byte matches or mismatches the byte value (Col 134, lines 31-33. Test passes or fails.).

5. Carron teaches substantial features of the claimed invention including instructions for comparing a byte in a register with a specified value (Col 39, lines 25-28), comparing a byte in a buffer with a specified byte value and performing branch instruction based on the comparison.

However, Carron does not teach a branch instruction that causes a processor to compare and branch based on a byte specified by the branch instruction; and of comparing a byte specified by the branch in instruction in a register and performing branching instructions based on the comparison.

6. White teaches of a processor executing a single instruction for performing compare and branch operations, wherein the branch/compare instruction specifies the sources for comparison. (Col 5, lines 25-43).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carron with the teachings of White with the motivation that the teachings of White for a processor instruction to perform both compare and branch operations, wherein the instruction specifies the sources for comparison would improve the efficiency of Carron's system by reducing the number of the instructions executed by the processor.

8. Yates teaches of executing branch instructions based on comparing a byte in a register with a specified value (Col 77, lines 29-33).

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Carron, White, and Yates with the motivation that the teachings of Yates to compare a byte value in a register and branch based on the comparison would improve the teachings of Carron by allowing the execution of instructions based on comparison of bytes values located not only in the buffer, but in other locations of the terminal.

10. As per claims 14, 17, and 20, Carron teaches substantially the invention as claimed including the method, processor, and program product for operating a processor, Carron's teachings comprise of:

executing a branch instruction by (Col 134, lines 8-12. Branch.):

a register stack (Col 39, lines 25-28; Col 40, lines 43-45. Register.).

an arithmetic logic unit coupled to the register stack and a program control store that stores a branch instruction that cues the processor to (Fig 3; Col 18, lines 10-15. Processor executes instructions. ALU is inherent. Col 7, lines 59-64. Instructions are stored in memory.):

fetch a byte stored in a buffer (Col 134, line 8. Byte from buffer.);

determine whether the byte in the buffer is equal or not equal to a specified byte value contained in the instruction (Col 134, lines 8-12. Compare byte with the value stored in the specified variable.); and

perform a branch operation specified by the branch instruction based on the specified byte being equal or not equal to the byte in the buffer (Col 134, lines 8-12. Branch if test passes.).

11. Carron teaches substantial features of the claimed invention including comparing a byte in a register with a specified value (Col 39, lines 25-28); and comparing a byte in a buffer with a specified byte value and performing a branch instruction based on the comparison (Col 134, lines 30-31). However, Carron does not teach of fetching a byte, specified by the branch instruction, stored in a register, specified by the branch instruction, and comparing the byte located in the register with a specified value to perform branching instructions.

12. White teaches of a processor executing a single instruction for performing compare and branch operations, wherein the branch/compare instruction specifies the sources for comparison. (Col 5, lines 25-43).

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carron with the teachings of White with the motivation that the teachings of White for a processor instruction to perform compare and branch operations, wherein the instruction specifies the sources for comparison would improve the efficiency of Carron's system by reducing the number of the instructions executed by the processor.

14. Yates teaches of executing branch instructions based on comparing a byte in a register with a specified value (Col 77, lines 29-33).

15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Carron and Yates because both teachings are similar in that they teach of executing branch instructions based on comparison of byte values. The teachings of Yates to compare a byte value in a register and branch based on the comparison would improve the teachings of Carron by allowing the terminal of Carron to execute instructions based on comparison of bytes values located not only in the buffer, but in other regions of the terminal.

16. As per claims 2, 15, 18, and 21, Carron teaches the invention wherein performing the branch instruction that causes the processor to perform the branching operation causes the process to branch to an instruction at a specified label (Col 118, lines 11-12. Branch to address label.).

17. As per claims 3, 16, and 19, Carron teaches the invention wherein branch instruction comprises: a bit_position field that specifies the byte in a longword contained in the register (Col 22, lines 39-52, Col 134, line 14-26. Indicates byte position, indicated by opcode commands.).

18. As per claim 6, Carron teaches the method of claim 1 wherein the register is a context-relative transfer register or a general-purpose register that holds the operand (Col 26, line 65-Col 27, line 2. Operation routines are stored in memory.).

19. As per claim 10, Carron teaches the method of claim 1 wherein the branch instruction allows branches to occur based on evaluation of a byte that is in a data path of a processor (Col 134, lines 8-12. Branching occurs of byte in buffer.).

20. As per claim 13, Carron teaches the method of claim 1 wherein the branch instruction includes a Byte_spec Number that specifies the byte in the register to be compared with byte_compare_value (Col 39, lines 25-29; Col 134, lines 23-25. Instruction specifies the byte to be compared with the variable. ).

21. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carron, White, and Yates, in view of Atkins et al, US Patent #5,898,866 (Atkins hereinafter).

22. As per claims 4 and 5, Carron does not teach the method of claim 1 wherein the branch instruction comprises: an optional token that is set by a programmer and specifies a number i of instructions to execute following the branch instruction before performing the branch operation where the number of instruction before performing the branch operation where the number of instructions can be specified as one, two, or three.

23. Atkin teaches of an implementing hardware to execute loops for a branch operation, wherein a field in the instruction specifies the number of instructions to execute prior to branching (Col 2, lines 28-31; Col 10, lines 21-23.).

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Carron and Atkins with the motivation that the teachings of Atkin's to specific the number of instructions prior to branching would enhance the system of Carron, White, and Yates by reducing code space and decreasing execution time.

25. Claims 7, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carron, White, and Yates, in view of Bruckert et al, US Patent #4,742,151 (Bruckert hereinafter).

26. As per claims 7 and 8, Carron taught of instructions to execute following the branch instruction before performing the branch operation (Col 134, lines 8-26). However, Carron does not teach the method wherein the branch instruction comprises: an optional token that is set by a programmer and which specifies a guess_branch prefetch for the instruction for the "branch taken" condition rather than the next sequential instruction.

27. Brucket teaches of executing instructions where a determination is made as to whether a branch should or should not be taken, and teaches of prefetching "branch taken " instructions (Col 1, lines 22-29).

28. It would have been obvious to one of ordinary skill in the art the time the invention was made to combine the teachings of Carron and Brucket with the motivation that all the teachings deal with executing branching instructions in a processing system and the teachings of Brucket

to prefetch "branch taken" instructions and executing branch guessing instructions would improve the system of Carron, White, and Yates by allowing high instruction throughput.

29. As per claim 11, Carron taught the method of claim 1 wherein the branch instruction branches on a byte matching the byte value (Col 134, lines 8-10). However, Carron does not teach wherein instruction prefetches the instruction for the "branch taken" condition.

30. Brucket teaches of executing instructions where a determination is made as to whether a branch should or should not be taken, and teachings of prefetching "branch taken " instructions (Col 1, lines 22-29).

31. It would have been obvious to one of ordinary skill in the art the time the invention was made to combine the teachings of Carron and Brucket with the motivation that the teachings of Brucket to prefetch "branch taken" instructions and executing branch guessing instructions would improve the system of Carron, White, and Yates by allowing high instruction throughput.

32. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carron, White, and Yates, in view of Gusefski et al, US Patent #5,202,972 (Gusefski hereinafter).

33. As per claim 9, Carron does not teach the method of claim 1 wherein the branch instruction allows a programmer to specify which bit of the register to use to determine the branch operation.

34. Gusefski teaches a computer system executing branch operations, where the hardware allows the selection of bits from the registers to determine the branch operation (Col 7, lines 33-36).

35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teachings of Carron and Gusefski with the motivation that the teachings of Gusefski to allow for the selection of the bit of the register to use for the branch operation would improve the teachings of Carron, White, and Yates by increasing the capability of the programmer to control the branching processes.

36. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carron, White, and Yates in view of Rodriguez, US Patent #6,139,199 (Rodriguez hereinafter).

37. As per claim 12, Carron does not teach the method of claim 1 wherein the branch instruction branches on a byte not matching the byte value and wherein the instruction prefetches the next sequential instruction.

38. Yates teaches of performing a branch instruction if the byte contained in the register is not equal to a specified value (Col 77, lines 29-33).

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Carron and Yates with the motivation that the teachings of Yates to execute branching when the bytes do not match would improve the system of Carron, White, and Yates by allowing for the continuation of executing instructions in conditional processing.

40. Rodriguez teaches of prefetching instructions (Col 12, lines 49-57).

41. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Carron, White, Yates, and Rodriguez with the motivation that

the teachings of Rodriguez to prefetch instructions would improve the system of Carron, White, and Yates by ensuring that the execution units are performing operations, which would reduce the time required to process instructions.

***Conclusion***

42. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i) Lee et al, US Patent #4,755,966, discloses a compare and branch instruction that specifies source register address fields for comparison.

ii) Beard et al, US Patent #5,544,337, discloses a branch instruction that includes compare code.

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

44. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Joo whose telephone number is 571 272-3966. The examiner can normally be reached on Monday to Friday 7 to 4.

46. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on 571 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

47. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 6, 2006
JJ

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